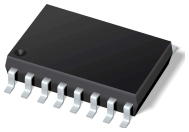




# QUAD DIFFERENTIAL PECL RECEIVERS

## FEATURES

- **Low-Voltage Functional Replacements for the Agere BRF1A, BRF2A, BRS2A, and BRS2B**
- **Pin-Equivalent to General Trade 26LS32 Devices**
- **High-Input Impedance Approximately 8 kΩ**
- **3.5-ns Maximum Propagation Delay**
- **TB3R1 Provides 50-mV Hysteresis**
- **TB3R2 With -125-mV Threshold Offset for Preferred State Output**
- **-0.5-V to 5.2-V Common Mode Range**
- **Single 3.3 V 10% Supply**
- **Slew Rate Limited (0.5 ns min 80% to 20%)**
- **TB3R2 Output Defaults to Logic 1 When Inputs Left Open or Shorted to $V_{CC}$ or GND**
- **ESD Protection HBM > 3 kV, CDM > 2 kV**
- **Operating Temperature Range: -40°C to 85°C**
- **Available SOIC (D) Package**

## APPLICATIONS

- **Digital Data or Clock Transmission Over Balanced Lines**

## DESCRIPTION

These quad differential receivers accept digital data over balanced transmission lines. They translate differential input logic levels to TTL output logic levels.

The TB3R1 is a pin- and function-compatible replacement for the Agere Systems BRF1A and BRF2A; it includes 3-kV HBM and 2-kV CDM ESD protection.

The TB3R2 is a pin- and function-compatible replacement for the Agere Systems BRS2A and BRS2B and incorporates a -125-mV receiver input offset, preferred state output, 3-kV HBM and 2-kV CDM ESD protection. The TB3R2 preferred state feature places the output in the high state when the inputs are open, shorted to ground, or shorted to the power supply.

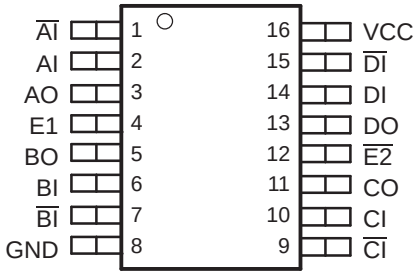
The power-down loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence they do not load the transmission line when the circuit is powered down.

The package for these differential line receivers is the 16-pin SOIC (D) package.

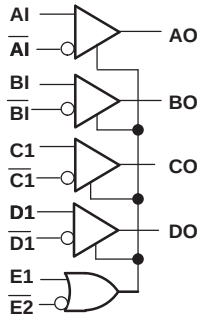
The enable inputs of this device include internal pullup resistors of approximately 40 kΩ that are connected to $V_{CC}$ to ensure a logical high level input if the inputs are open circuited.

### PIN ASSIGNMENTS

**D PACKAGE**
**(TOP VIEW)**




### FUNCTIONAL BLOCK DIAGRAM




### Enable Truth Table

| E1 | $\overline{E2}$ | CONDITION |
|---|---|---|
| 0 | 0 | Active |
| 1 | 0 | Active |
| 0 | 1 | Disabled |
| 1 | 1 | Active |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003–2008, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| PART NUMBER | PART MARKING | Package | LEAD FIISH | STATUS |
|---|---|---|---|---|
| TB3R1D | TB3R1 | SOIC | NiPdAu | Production |
| TB3R2D | TB3R2 | SOIC | NiPdAu | Production |

## POWER DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | POWER RATING $T_A \leq 25°C$ | THERMAL RESISTANCE, JUNCTION-TO-AMBIENT WITH NO AIR FLOW | DERATING FACTOR(1) $T_A \geq 25°C$ | POWER RATING $T_A = 85°C$ |
|---|---|---|---|---|---|
| D | Low-K(1) | 763 mW | 131.1°C/W | 7.6 mW/°C | 305 mW |
| | High-K(2) | 1190 mW | 84.1°C/W | 11.9 mW/C | 475 mW |
| DW | Low-K(1) | 831 mW | 120.3°C/W | 8.3 mW/°C | 332 mW |
| | High-K(2) | 1240 mW | 80.8°C/W | 12.4 mW/°C | 494 mW |

(1) In accordance with the low-K thermal metric definitions of EIA/JESD51-3.
(2) In accordance with the high-K thermal metric definitions of EIA/JESD51-7.

## THERMAL CHARACTERISTICs

| PARAMETER | | PACKAGE | VALUE | UNIT |
|---|---|---|---|---|
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | D | 47.5 | °C/W |
| | | DW | 53.7 | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | D | 44.2 | °C/W |
| | | DW | 47.1 | °C/W |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | | | 0 V to 6 V |
| Magnitude of differential bus (input) voltage, $\lvert V_{AI} - V\rvert$, $\lvert V_{BI} - V\rvert$, $\lvert V_{CI} - V\rvert$, $\lvert V_{DI} - V\rvert$ | | | 6.5 V |
| ESD | Human Body Model(2) | All pins | 3 kV |
| | Charged-Device Model(3) | All pins | 2 kV |
| Continuous power dissipation | | | See Dissipation Rating Table |
| Storage temperature, $T_{stg}$ | | | -65°C to 150°C |

(1) Stresses beyond those listed under„ absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.


Copyright © 2003–2008, Texas Instruments Incorporated

## RECOMMENDED OPERATING CONDITIONS

| | MIN | Nom | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3 | 3.3 | 3.6 | V |
| Bus pin input voltage, $V_{AI}$, V, $V_{BI}$, V, $V_{CI}$, V, $V_{DI}$, V | -0.6(1) | | 5.3 | V |
| Magnitude of differential input voltage, $\|V_{AI}$ - V$\|$, $\|V_{BI}$ - V$\|$, $\|V_{CI}$ - V$\|$, $\|V_{DI}$ - V$\|$ | 0.1 | | 5 | V |
| Operating free-air temperature, $T_A$ | -40 | | 85 | C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet, unless otherwise noted.

## DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current(1) | Outputs disabled | | | 34 | mA |
| | | Outputs enabled | | | 32 | mA |

(1) Current is dc power draw as measured through GND pin and does not include power delivered to load.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

| parameter | | test conditions | | min | typ | max | unit |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output low voltage | $V_{CC}$ = 3 V, | $I_{OL}$ = 8 mA | | | 0.4 | V |
| $V_{OH}$ | Output high voltage | $V_{CC}$ = 3 V, | $I_{OH}$ = -400 A | 2.4 | | | V |
| $V_{IL}$ | Low level enable input voltage(1) | $V_{CC}$ = 3.6 V | | | | 0.8 | V |
| $V_{IH}$ | High level enable input voltage(1) | $V_{CC}$ = 3.6 V | | 2 | | | V |
| $V_{IK}$ | Enable input clamp voltage | $V_{CC}$ = 3 V, | $I_I$ = -5 mA | | | -1(2) | V |
| $V_{TH+}$ | Positive-going differential input threshold voltage(1), ($V_{xI}$ - V) | x = A, B, C, or D | TB3R1 | | | 100 | mV |
| | | | TB3R2(3) | | | -50 | mV |
| $V_{TH-}$ | Negative-going differential input threshold voltage(1), ($V_{xI}$ - V) | x = A, B, C, or D | TB3R1 | | | -100(2) | mV |
| | | | TB3R2(3) | | | -200(2) | mV |
| $V_{HYST}$ | Differential input threshold voltage hysteresis, ($V_{TH+}$ - $V_{TH\_}$) | TB3R1 | | | 50 | | mV |
| $I_{OZL}$ | Output off-state current, (High-Z) | $V_{CC}$ = 3.6 V | $V_O$ = 0.4 V | | | -20(2) | A |
| $I_{OZH}$ | | | $V_O$ = 2.4 V | | | 20 | A |
| $I_{OS}$ | Output short circuit current(4) | $V_{CC}$ = 3.6 V | | | | -100(2) | mA |
| $I_{IL}$ | Enable input low current | $V_{CC}$ = 3.6 V, | $V_{IN}$ = 0.4 V | | | -400(2) | A |
| $I_{IH}$ | Enable input high current | $V_{CC}$ = 3.6 V | $V_{IN}$ = 2.7 V | | | 20 | A |
| | Enable input reverse current | | $V_{IN}$ = 3.6 V | | | 100 | A |
| $II_L$ | Differential input low current | $V_{CC}$ = 3.6 V, | $V_{IN}$ = -1.2 V | | | -2(2) | mA |
| $I_{IH}$ | Differential input high current | $V_{CC}$= 3.6 V, | $V_{IN}$ = 5.3 V | | | 1 | mA |
| $R_O$ | Output resistance | | | | 20 | | Ω |

(1) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.
(2) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(3) Outputs of unused receivers assume a logic 1 level when the inputs are left open. (It is recomended that all unused positive inputs be tied to the positive power supply. No external series resistor is required.)
(4) Test must be performed one lead at a time to prevent damage to the device.

Copyright © 2003–2008, Texas Instruments Incorporated

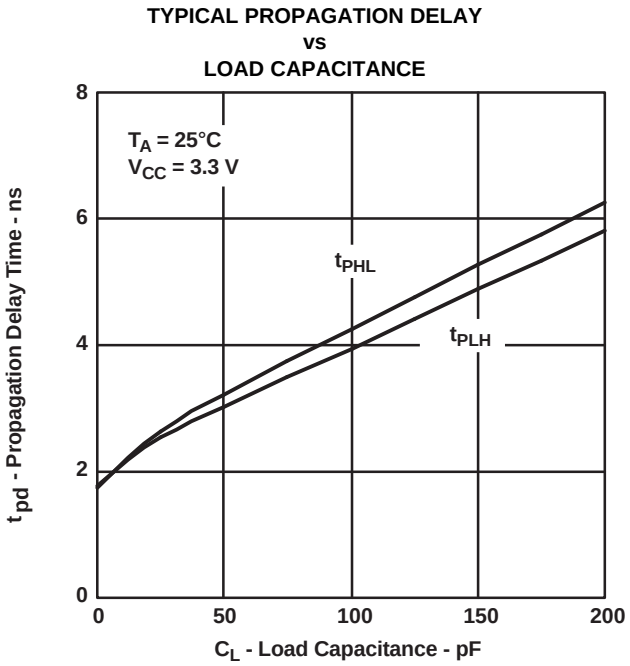
## SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

| parameter | | test conditions | min | typ | max | unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 0 pF(1), See Figure 2 and Figure 4 | | 1.8 | 3.5 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 1.8 | 3.5 | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $C_L$ = 15 pF, See Figure 2 and Figure 4 | | 2.3 | 4 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 2.3 | 4 | |
| $t_{PHZ}$ | Output disable time, high-level-to-high-impedance output(2) | $C_L$ = 5 pF See Figure 3 and Figure 5 | | 4.4 | 12 | ns |
| $t_{PLZ}$ | Output disable time, low-level-to-high-impedance output(2) | | | 3.3 | 12 | ns |
| $t_{skew1}$ | Pulse width distortion, $\lvert t_{PHL} - t_{PLH} \rvert$ | $C_L$ = 10 pF, See Figure 2 and Figure 4 | | | 0.7 | ns |
| | | $C_L$ = 150 pF, See Figure 2 and Figure 4 | | | 4 | ns |
| $\Delta t_{skew1p-p}$ | Part-to-part output waveform skew(3) | $C_L$ = 10 pF, $T_A$ = 75C, See Figure 2 and Figure 4 | | 0.8 | 1.4 | ns |
| | | $C_L$ = 10 pF, $T_A$ = -40C to 85C, See Figure 2 and Figure 4 | | | 1.5 | ns |
| $\Delta t_{skew}$ | Same part output waveform skew(3) | $C_L$ = 10 pF, See Figure 2 and Figure 4 | | | 0.3 | ns |
| $t_{PZH}$ | Output enable time, high-impedance-to-high-level output(2) | $C_L$ = 10 pF, See Figure 3 and Figure 4 | | 6 | 12 | ns |
| $t_{PZL}$ | Output enable time, high-impedance-to-low-level output(2) | | | 4 | 12 | ns |
| $t_{TLH}$ | Rise time (20%-80%) | $C_L$ = 10 pF, See Figure 2 and Figure 4 | 0.5 | | 2 | ns |
| $t_{THL}$ | Fall time (80%-20%) | | 0.5 | | 2 | ns |

(1) The propagation delay values with a 0 pF load are based on design and simulation.
(2) See Table 1.
(3) Output waveform skews are when devices operate with the same supply voltage, same temperature, have the same packages and the same test circuits.

## TYPICAL CHARACTERISTICS




A. NOTE: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to external capacitance and the intrinsic delay of the device. Intrinsic delay is listed in the table above as the 0 pF load condition. The incremental increase in delay between the 0 pF load condition and the actual total load capacitance represents the extrinsic, or external delay contributed by the load.

**Figure 1. Typical Propagation Delay vs Load Capacitance at 25C**


Copyright © 2003–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS (continued)

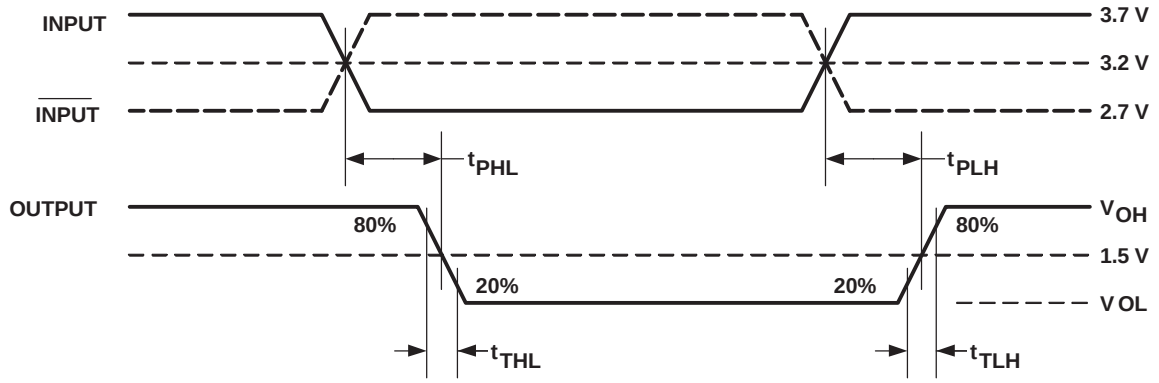
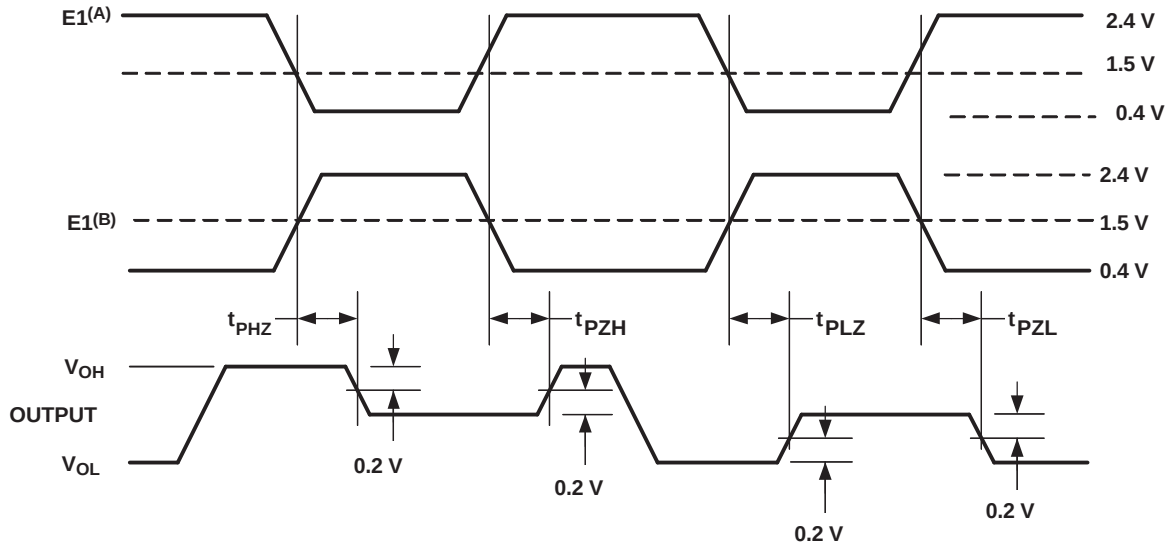



**Figure 2. Receiver Propagation Delay Times**

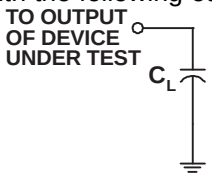



A. $\overline{E2}$ = 1 while E1 changes states.

B. E1 = 0 while $\overline{E2}$ changes states.

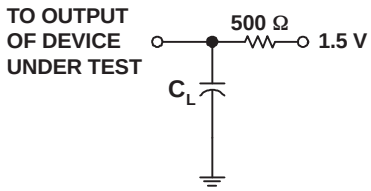
**Figure 3. Receiver Enable and Disable Timing**

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.




$C_L$ includes test-fixture and probe capacitance.

**Figure 4. Receiver Propagation Delay Time and Enable Time ($t_{PZH}$, $t_{PZL}$) Test Circuit**




$C_L$ includes test-fixture and probe capacitance.

**Figure 5. Receiver Disable Time ($t_{PHZ}$, $t_{PLZ}$) Test Circuit**

Copyright © 2003–2008, Texas Instruments Incorporated

## TYPICAL CHARACTERISTICS (continued)

LOW-TO-HIGH PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

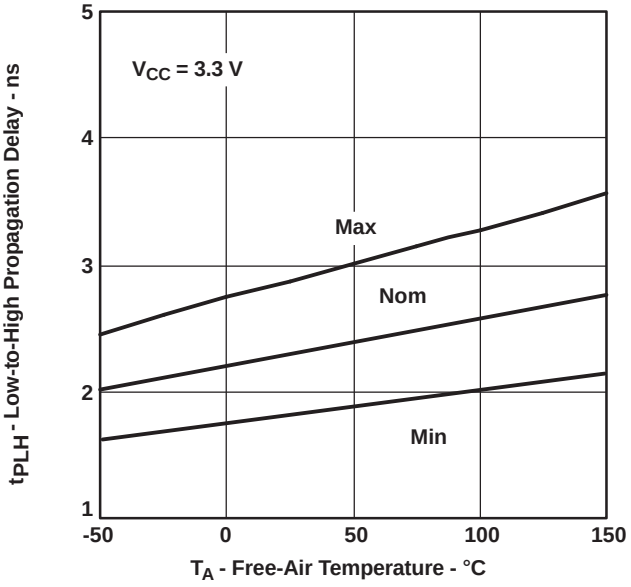



Figure 6.

HIGH-TO-LOW PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

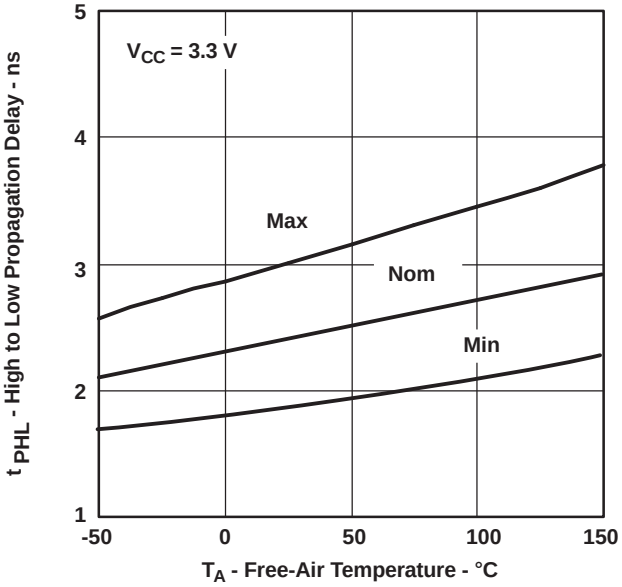



Figure 7.

MINIMUM $V_{OH}$ AND MAXIMUM $V_{OL}$
vs
FREE-AIR TEMPERATURE

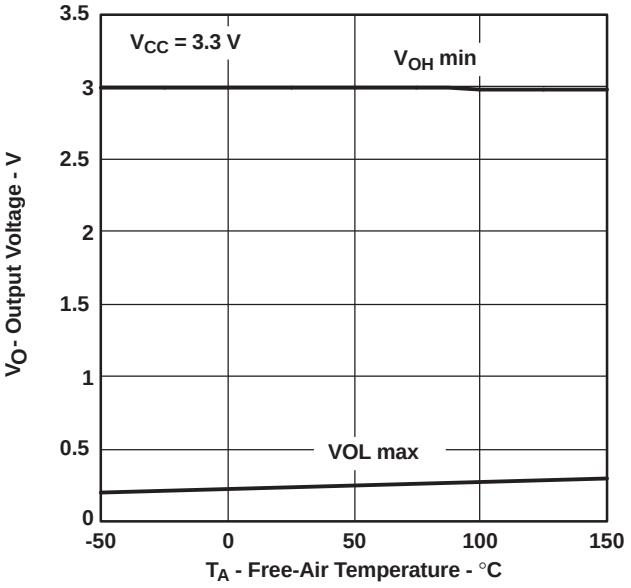



Figure 8.

TYPICAL AND MAXIMUM $I_{CC}$
vs
FREE-AIR TEMPERATURE

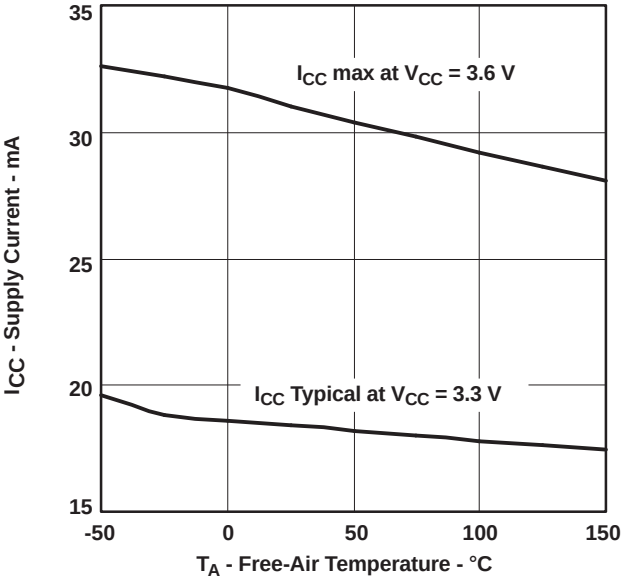



Figure 9.


Copyright © 2003–2008, Texas Instruments Incorporated

## APPLICATION INFORMATION

### Power Dissipation

The power dissipation rating, often listed as the package dissipation rating, is a function of the ambient temperature, $T_A$, and the airflow around the device. This rating correlates with the device's maximum junction temperature, sometimes listed in the absolute maximum ratings tables. The maximum junction temperature accounts for the processes and materials used to fabricate and package the device, in addition to the desired life expectancy.

There are two common approaches to estimating the internal die junction temperature, $T_J$. In both of these methods, the device internal power dissipation $P_D$ needs to be calculated This is done by totaling the supply power(s) to arrive at the system power dissipation:

$$\sum(V_{Sn} \times I_{Sn}) \quad (1)$$

and then subtracting the total power dissipation of the external load(s):

$$\sum(V_{Ln} \times I_{Ln}) \quad (2)$$

The first $T_J$ calculation uses the power dissipation and ambient temperature, along with one parameter: $\theta_{JA}$, the junction-to-ambient thermal resistance, in degrees Celsius per watt.

The product of $P_D$ and $\theta_{JA}$ is the junction temperature rise above the ambient temperature. Therefore:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

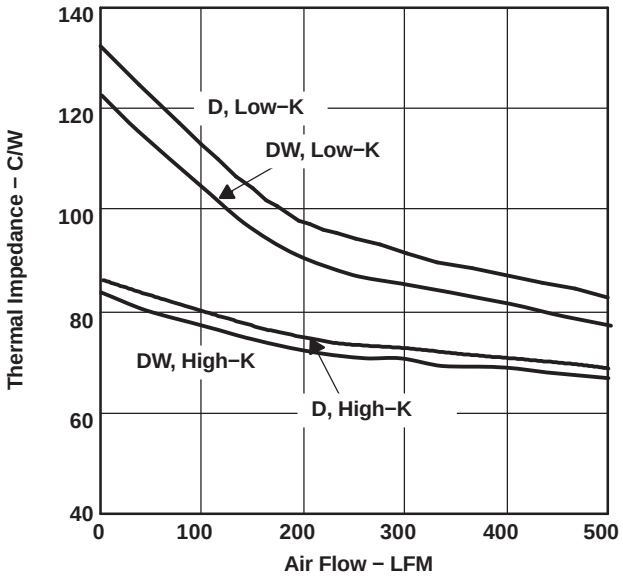



**Figure 10. Thermal Impedance vs Air Flow**

Note that $\theta_{JA}$ is highly dependent on the PCB on which the device is mounted, and on the airflow over the device and PCB. JEDEC/EIA has defined standardized test conditions for measuring $\theta_{JA}$. Two commonly used conditions are the low-K and the high-K boards, covered by EIA/JESD51-3 and EIA/JESD51-7 respectively. Figure 10 shows the low-K and high-K values of $\theta_{JA}$ versus air flow for this device and its package options.

The standardized $\theta_{JA}$ values may not accurately represent the conditions under which the device is used. This can be due to adjacent devices acting as heat sources or heat sinks, to nonuniform airflow, or to the system PCB having significantly different thermal characteristics than the standardized test PCBs. The second method of system thermal analysis is more accurate. This calculation uses the power dissipation and ambient temperature, along with two device and two system-level parameters:

- $\theta_{JC}$, the junction-to-case thermal resistance, in degrees Celsius per watt
- $\theta_{JB}$, the junction-to-board thermal resistance, in degrees Celsius per watt
- $\theta_{CA}$, the case-to-ambient thermal resistance, in degrees Celsius per watt
- $\theta_{BA}$, the board-to-ambient thermal resistance, in degrees Celsius per watt.

In this analysis, there are two parallel paths, one through the case (package) to the ambient, and another through the device to the PCB to the ambient. The system-level junction-to-ambient thermal impedance, $\theta_{JA(S)}$, is the equivalent parallel impedance of the two parallel paths:

$$T_J = T_A + \left(P_D \times \theta_{JA(S)}\right) \quad (4)$$

where

$$\theta_{JA(S)} = \frac{\left[\left(\theta_{JC} + \theta_{CA}\right) \times \left(\theta_{JB} + \theta_{BA}\right)\right]}{\left(\theta_{JC} + \theta_{CA} + \theta_{JB} + \theta_{BA}\right)} \quad (5)$$

The device parameters $\theta_{JC}$ and $\theta_{JB}$ account for the internal structure of the device. The system-level parameters $\theta_{CA}$ and $\theta_{BA}$ take into account details of the PCB construction, adjacent electrical and mechanical components, and the environmental conditions including airflow. Finite element (FE), finite difference (FD), or computational fluid dynamics (CFD) programs can determine $\theta_{CA}$ and $\theta_{BA}$. Details on using these programs are beyond the scope of this data sheet, but are available from the software manufacturers.

Copyright © 2003–2008, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TB3R1D | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R1DE4 | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R1DR | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R1DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R2D | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R2DE4 | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R2DR | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |
| TB3R2DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1YEAR/ Level-1-220C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

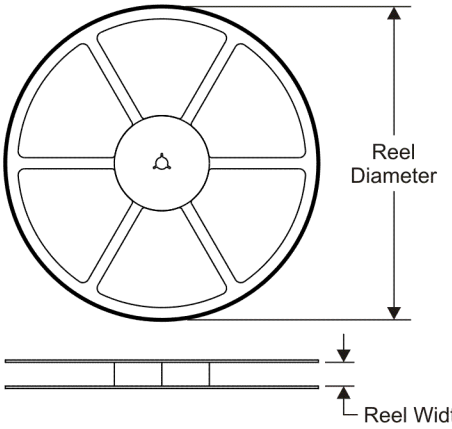
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

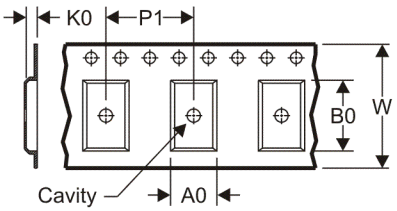
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

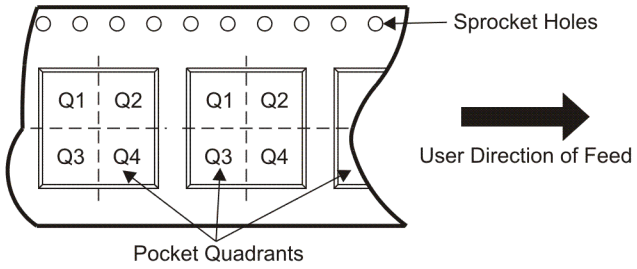



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

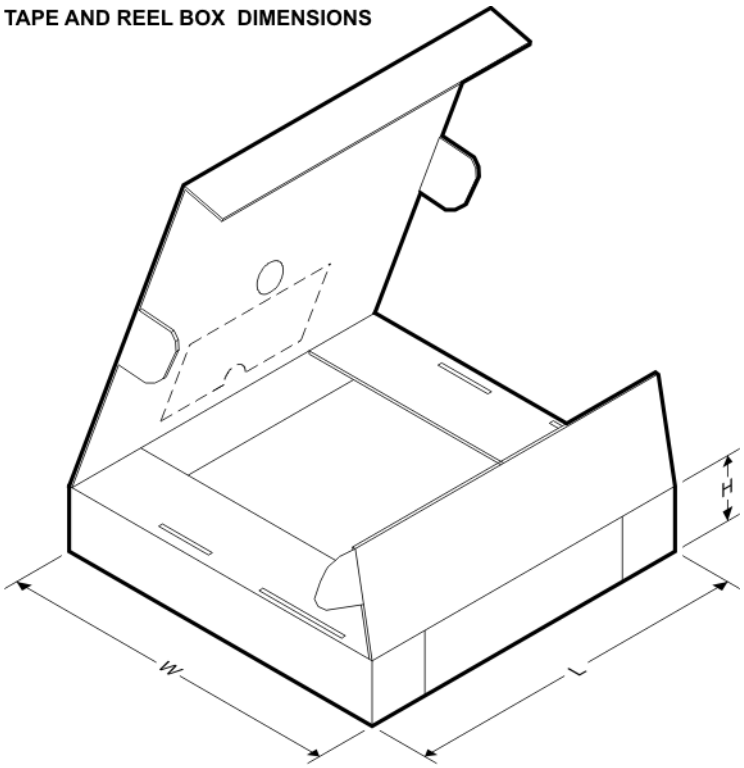
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TB3R1DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TB3R2DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

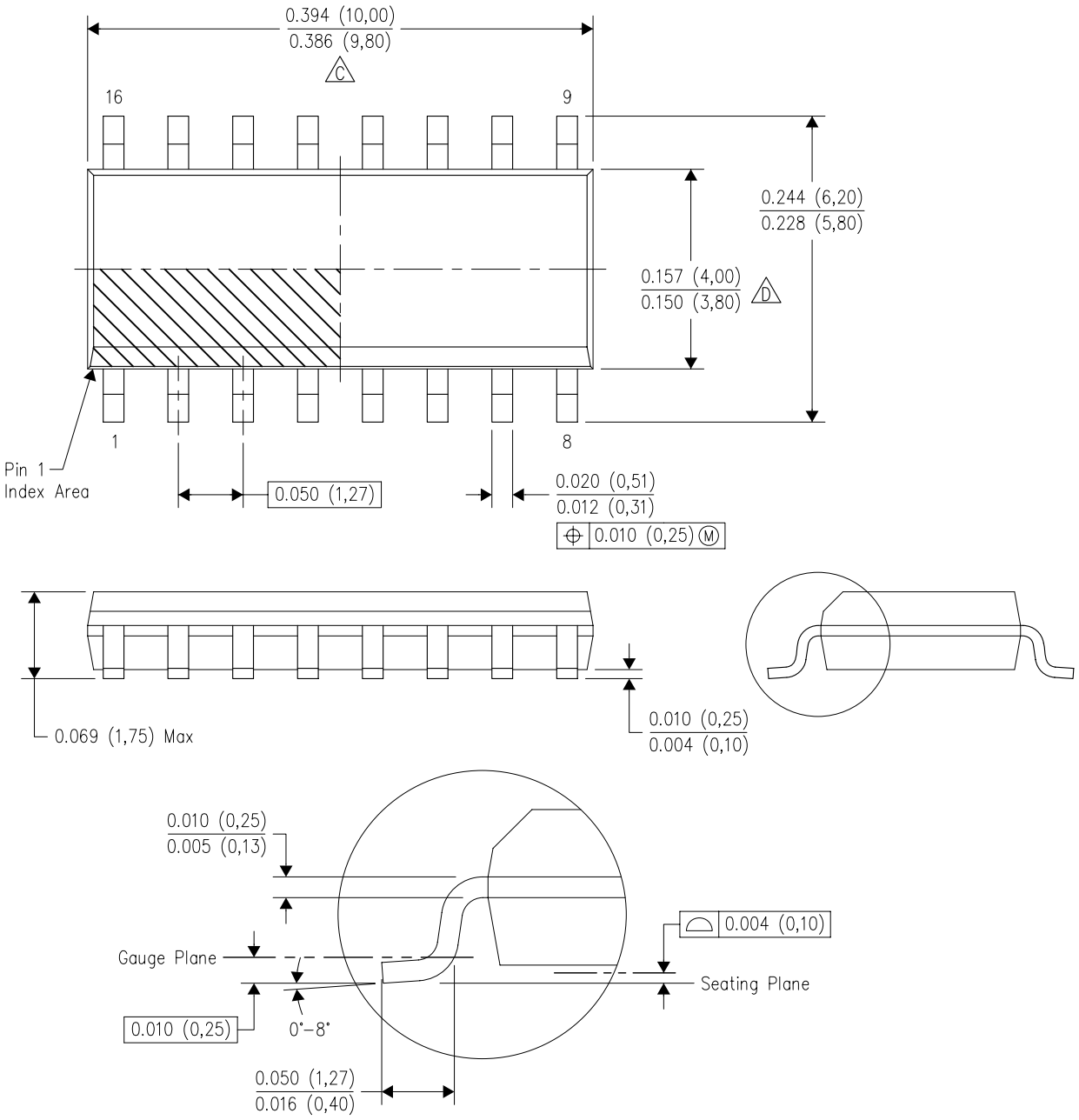
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

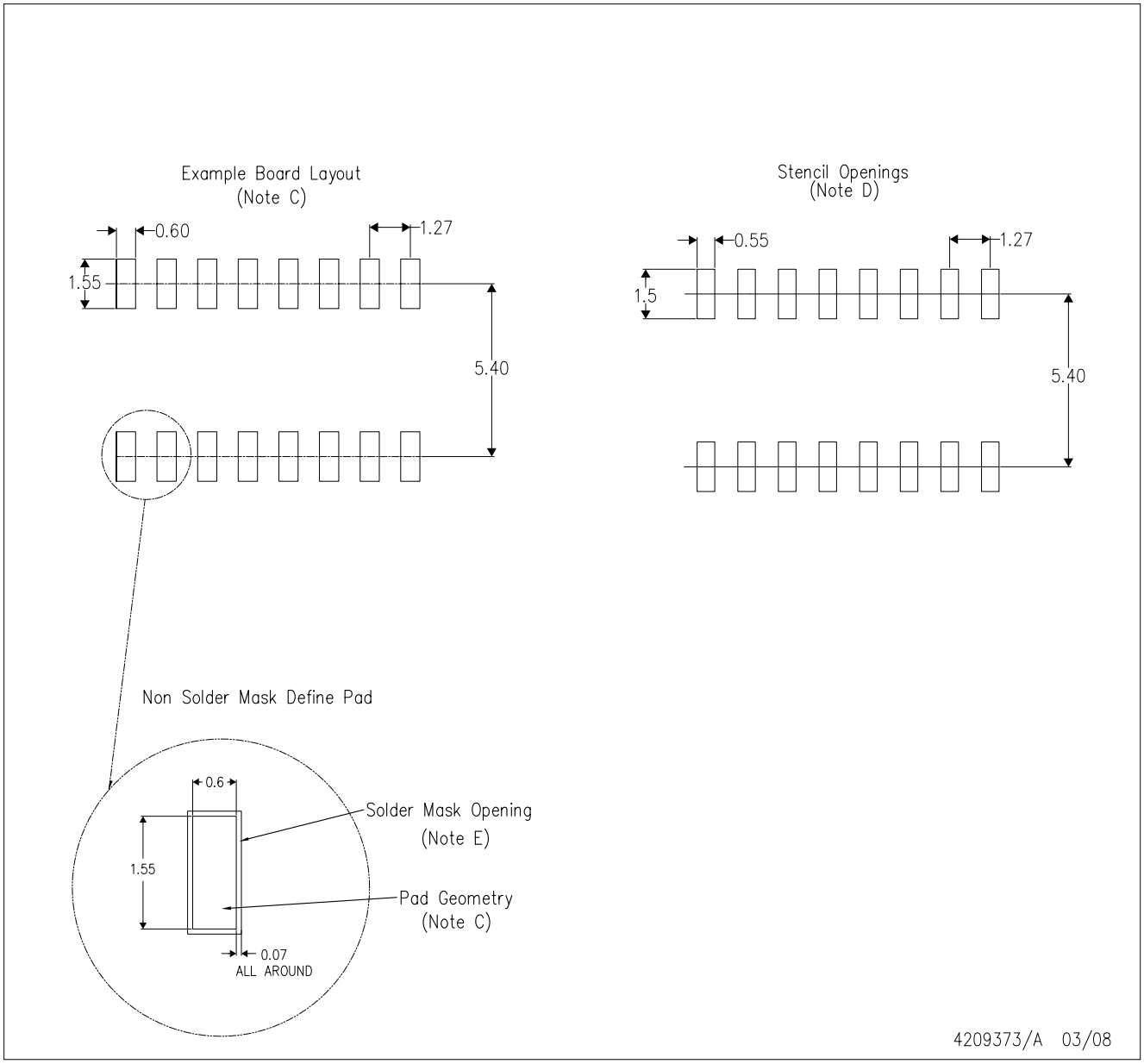
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TB3R1DR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |
| TB3R2DR | SOIC | D | 16 | 2500 | 346.0 | 346.0 | 33.0 |

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Clocks and Timers | www.ti.com/clocks | Digital Control | www.ti.com/digitalcontrol |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated